

## **APPENDIX B**

### **Low Residue Soldering Task Force (LRSTF) Printed Wiring Assembly (PWA)**

## **B.1 DESIGN OF THE LOW RESIDUE SOLDERING TASK FORCE (LRSTF) PRINTED WIRING ASSEMBLY**

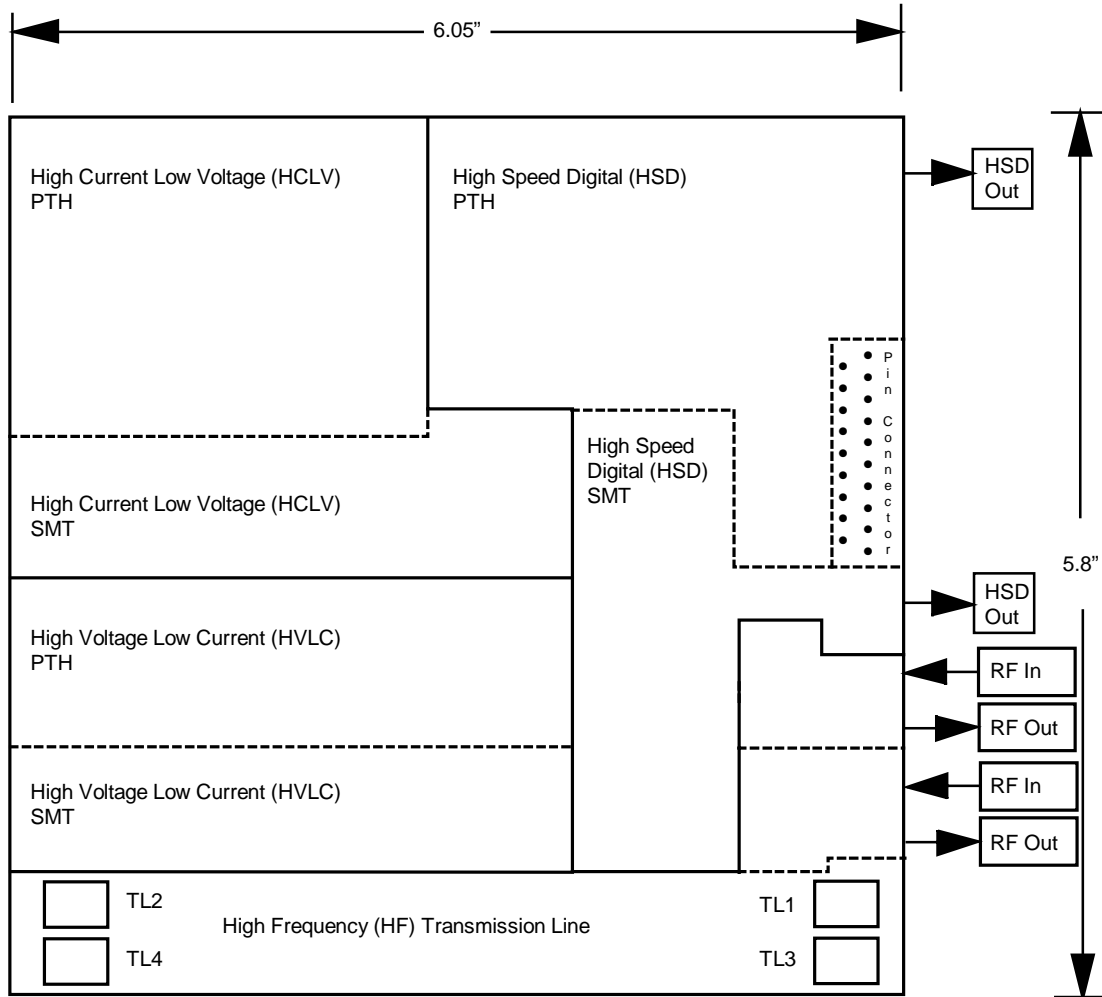
The primary test vehicle used in the LRSTF evaluation of low-residue technology was an electrically functional printed wiring assembly (PWA). This assembly was designed at Sandia National Laboratories in Albuquerque, NM based on input from LRSTF members and input received during open review meetings held by the task force.

The PWA measures 6.05 inches x 5.8 inches x 0.062 inches and is divided into seven sections, each containing one of the following types of electronic circuits:

- High Current, Low Voltage (HCLV)
- High Voltage, Low Current (HVLC)
- High Speed Digital (HSD)
- High Frequency Low Pass Filter(LPF)
- High Frequency Transmission Line Coupler (TLC)
- Other Networks (ON)
- Stranded Wire (SW).

The layout of the LRSTF functional assembly is shown in Figure B-1. Each quadrant of the PWA has subsections for PTH and SMT components, with each forming separate electrical circuits. The PWA includes a large common ground plane, components with heat sinks, and mounted hardware.

Each subsection shown contains both functional and nonfunctional components (added to increase component density). A 29-pin PTH edge connector is used for circuit testing. High frequency connectors are used to ensure proper impedance matching and test signal fidelity as required. Board fabrication drawings, schematics, and a complete listing of all components are available in separate cover.



**Figure B-1. Layout of the PWA Illustrating the Four Major Sections and Subsections**

## B.2 HIGH CURRENT, LOW VOLTAGE (HCLV)

The HCLV section of the board is in the upper left-hand corner of LRSTF PWA (see Figure B-1). The upper left-hand portion of this quadrant contains PTH components with SMT components immediately beneath.

### Purpose of the HCLV Experiment

Performance of high-current circuits is affected by series resistance. Resistance of a conductor (including solder joints) is determined by the following equation:

$$R = \frac{\rho L}{A_c} \text{ ohms}(\Omega) \quad (\text{B.1})$$

where  $\rho$  = resistivity, the proportionality constant  
L = length of the conductor  
 $A_c$  = cross-sectional area of the conductor (solder joints).

Resistance is most likely to change due to cracking or corrosion of the solder joint that may be related to the soldering process. These conditions decrease the cross-sectional area of the solder joints, thus increasing resistance as shown in Equation B.1. Use of high current to test solder joint resistance makes detection of a change in resistance easier.

A 5 Amperes (A) current has been selected as a value that would cover most military applications. A change of resistance is most conveniently determined by measuring the steady-state performance of the circuit, which will now be discussed.

### Steady State Circuit Performance.

Overall circuit resistance,  $R_{total}$ , is the parallel combination of the seven resistors,  $R_1$ ,

$R_2, \dots, R_7$ , (all resistors =  $10\Omega$ ) used in the HCLV circuit:

$$\frac{1}{R_{total}} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_2} + \dots + \frac{1}{R_7} = \frac{7}{10\Omega} \quad (\text{B.2})$$

$$R_{total} = \frac{10\Omega}{7} \quad (\text{B.3})$$

Since a current (I) of 5A will be applied to the circuit, the resulting voltage (V), according to Ohm's Law, is:

$$V = IR = 5A \times \frac{10\Omega}{7} = 7.14V \quad (\text{B.4})$$

Changes in resistance are thus detected by changes in voltage. However, a pulse width had to be chosen that would not overstress the circuit components. With current equally divided among the seven parallel resistors, the power (P) dissipated in each resistor, according to Joule's Law, is:

$$P = I^2 R = \left| \frac{5A}{7} \right|^2 \times 10\Omega = 5.1Watts(W) \quad (B.5)$$

Since the power rating for the PTH wire-wound resistor is 3W, the rating is exceeded by a factor of 1.7 for steady state (5.1 / 3). Design curves from the resistor manufacturer indicate the PTH wire-wound resistors could tolerate the excess power for about 100 *ms*. The SMT resistors are rated at 1W, so the steady state rating is exceeded by a factor of five. With the manufacturer unable to provide the pulse current capability of the SMT resistors, a pulse derating factor could not be determined. A pulse width of 100  $\mu s$  was selected, which is three orders of magnitude less than the capability of the wire-wound resistors. This width is also sufficiently long for the circuit to achieve steady state before the measurement is taken.

### Circuit Board Design

Traces carrying the 5A current were placed on an inner layer of the circuit board because: (1) the primary concern was the possible degradation of the solder connections as discussed above, and (2) the bulk electrical characteristics (resistivity) of the traces should not be affected by flux residues. High-current trace widths were designed to be 250 mils whenever possible (following MIL-STD-275). This width with a 5A current should cause no more than a 30°C temperature rise under steady-state conditions.

The resistor and capacitor values were selected to be readily available. If other values are used, care should be taken to not over-stress the parts, as discussed above.

### B.3. HIGH VOLTAGE LOW CURRENT

The HVLC circuitry is immediately below the HCLV circuitry and above the high-frequency transmission lines. The PTH circuitry is in the upper part of this subsection with the SMT circuitry beneath.

#### Purpose of the HVLC Experiment

Flux residues could decrease the insulation resistance between conductors. The impact of this decrease could be significant in circuits with a high-voltage gradient across the insulating region. Decreased resistance can be detected by an increase in current when a high voltage is applied to the circuit. A voltage of 250V was selected as the high potential for this test. The change in leakage current is determined by measuring the steady-state performance of the circuit, which will now be discussed.

#### Steady State Circuit Performance

Steady-state operation of the HVLC circuit can be determined by considering only the resistors. The total resistance of the series combination is the sum of the resistances:

$$R_{total} = R_1 + R_2 + R_3 + R_4 = R_5 = 50M\Omega \quad (B.6)$$

since all resistors are 10M $\Omega$  each.

From Ohm's law, the current flowing into the circuit with 250V applied is:

$$I = \frac{V}{R} = \frac{250V}{50M\Omega} = 5\mu A \quad (B.7)$$

Care was taken to not over-stress the individual components in the circuits. The voltage stress across each resistor-capacitor pair is one-fifth of the applied 250V, or 50V. The voltage ratings are 250V for the PTH resistors, 200V for the SMT resistors, and 250V for all the capacitors. Power rating is not a concern due to the low current.

#### Circuit Board Design

High voltage traces were placed next to ground potential traces by design. The spacings between the high voltage and intermediate traces were selected using MIL-STD-275 and were calculated as shown in Table B-1 below.

**Table B-1. Voltage per Trace Spacing**

Voltage	Spacing Between Traces (mils)
0 - 100	5
101 - 300	15
301 - 500	30

These guidelines were followed except the 5-mil spacing, where 10 mils was used to facilitate board fabrication. Table B-2 lists the voltage on various board circuit traces and the spacing to the adjacent ground trace.

Resistors and capacitors were selected to have readily available values — different values could have been used to achieve particular experimental goals. For instance, higher-resistance values could be used with lower-value capacitors. Reverse biased, low-leakage diodes could also be used for higher sensitivity to parasitic leakage resistance.

**Table B-2. HVLC Circuit Board Trace Potentials**

Technology	Trace Connected to:		Potential (V)	Trace Length at Potential (in)	Spacing (mils)
	Resistor	Capacitor			
PTH	R15	C21	250	0.8	30
			200	0.4	15
	R16	C22	200	0.4	15
			150	N/A	
	R17	C23	150	N/A	
			100	0.4	10
	R18	C24	100	0.4	10
			50	N/A	
	R19	C25	50	N/A	
SMT	R20	C26	250	5.0	30
			200	1.0	15
	R21	C27	200	1.0	15
			150	N/A	
	R22	C28	150	N/A	
			100	0.9	10
	R23	C29	100	0.9	10
			50	N/A	
	R24	C30	50	N/A	

N/A = Not Applicable since no 50V or 150V traces were adjacent to ground potential

#### **B.4. HIGH SPEED DIGITAL (HSD)**

The HSD circuitry is in the upper right-hand corner of the LRSTF PWA as shown in Figure B-1. This subsection contains the PTH circuitry and consists of two 14-pin dual in-line package (DIP) integrated circuits (ICs). The SMT subsection IC is a single 20-pin leadless chip carrier (LCC) package. Each of these ICs is a “fast” bi-polar digital “QUAD-DUAL-INPUT-NAND-GATE.” Both subsections contain two ceramic capacitors that bypass spurious noise on the power input line (VCC) to the ICs and an output high-frequency connector. Inputs to both subsections are applied through the edge-connector on the right side of the board. Figure B-2 shows a simplified schematic of the ICs.

##### Purpose of the HSD Experiment

The output signal of each gate in Figure B-2 is opposite in polarity to the input signal. If the traces of these two signals are in close proximity on the printed circuit board (capacitively coupled), the gate switching speed might be affected by the presence of flux residues. A 5 VDC bias will be applied to the VCC inputs during environmental testing to accelerate aging. One PTH IC (U02) will be hand soldered during assembly at each site to introduce hand solder flux residue in the experiment.

##### Circuit Description

The schematic in Figure B-2 represents the ICs in the PTH and SMT subsections. The ICs are random logic circuits that are NAND (Not AND) gates. An AND gate’s output is high only when all inputs are high. The logic of a NAND gate is opposite the logic of an AND gate. Therefore, the output of a NAND gate is low only when all inputs are high; otherwise, the output is high. With the two connected inputs, the output of each gate is opposite the input. Since the four gates are connected in series, the output of the last gate is the same logic level (high or low) as the input, with a slight lag.

The output pulse does not change logic levels instantaneously, but the switching times from low to high (rise time) and from high to low (fall time) should be less than 7ns. ICs should perform within these criteria if the VCC input is  $5 \pm 0.5V$  DC, the output load does not exceed specifications, and the circuit has a proper ground plane as shown in Figure B-2.

The HSD circuits also provide an intermediate test for high frequencies, with switching time dictating a high-frequency spectrum. The frequency spectrum of switching circuits can be expressed in terms of bandwidth (BW). For a switching circuit, the respective BWs (in Hertz) for rise ( $t_r$ ) and fall ( $t_f$ ) times are:

$$BW_r = \frac{0.35}{t_r} \text{ Hz} \quad \text{and} \quad BW_f = \frac{0.35}{t_f} \text{ Hz} \quad (\text{B.8})$$

Bipolar technology was used rather than a complementary metal oxide semiconductor (CMOS) since it is not as vulnerable to electrostatic discharge (ESD) damage. Available military bipolar technologies have typical switching speeds and bandwidths as indicated in Table B-3 below.

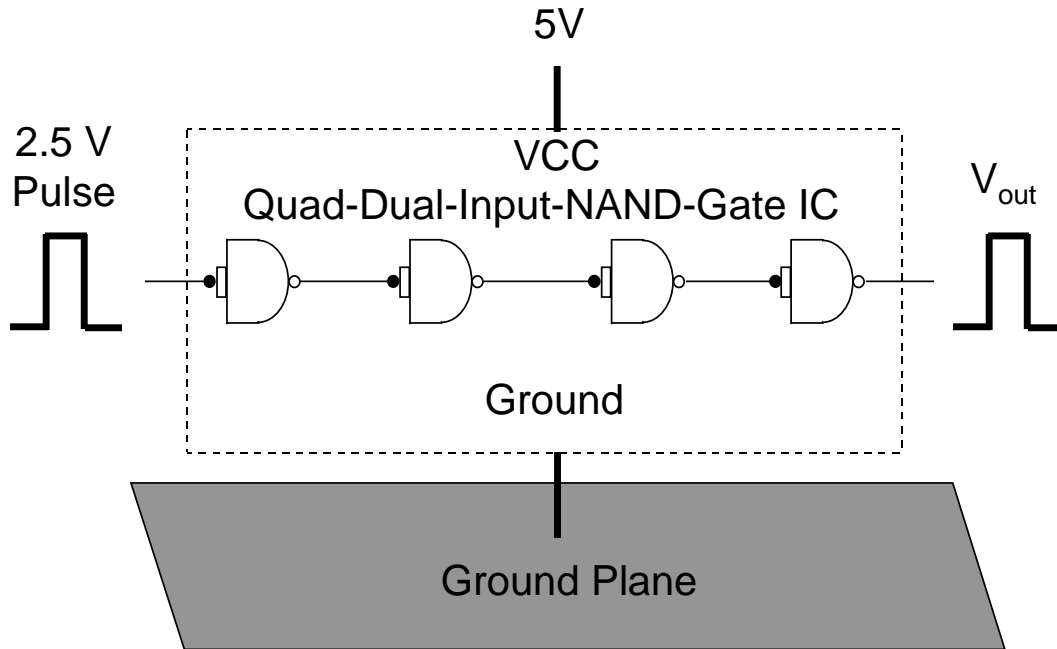
**Table B-3. Typical Switching Speeds and Bandwidths**

Technology	Typical $t_r$ or $t_f$	Bandwidth (MHz)
5404 TTL	12	29
54LS04 Low Power Schottky	9	39
54S04 Schottky	3	117
54F04 Advanced Schottky (Fast)	2.5	140

The Fast technology was selected since it had the shortest switching time and largest bandwidth, which provides the widest frequency spectrum for this test.

#### Circuit Board Design

Ground planes were provided for proper circuit operation of the ICs. The PTH subcircuit utilized the large common ground plane on layer 3 since most of the input and output traces are on layer 4. Since the SMT circuit traces are on the top layer, a smaller ground plane was added on layer 2. The “QUAD-DUAL-INPUT-NAND-GATE” was selected since other solder studies of national attention have used that particular type of IC, which makes direct comparisons with these studies possible. See Figure B-2.



**Figure B-2. Simplified Schematic of the ICs in the HSD Subsection**

## B.5. HIGH FREQUENCY (HF)

The HF section shown in the lower right-hand corner of Figure B-1 contains two major subsections, the low-pass filters (LPF) and the transmission line coupler (TLC). The TLC traces on layer 4 of the board are on the backside of the board. The LPF/PTH subsection is above the LPF/SMT subsection. Each of these subsections has discrete ceramic capacitors and three inductor-capacitor (LC) filters, with the inductor printed on the circuit board in a spiral pattern. The HF circuits allow evaluation of circuit performance up to 1GHz (1 GHz).

### Purpose of the High Frequency Experiment

Flux residues may affect the performance of LPF printed circuit inductors and transmission lines due to parasitic resistances and parasitic capacitances. These inductors will be purposely covered with flux during surface-mount solder processing to increase the presence of residues. Since the transmission lines are separated by only 10 mils, flux residues between the lines may affect their performance.

### LPF Circuit Description

An inductor-capacitor (LC) LPF consists of a series inductor followed by a shunt capacitor. A low-frequency signal passes through the LPF without any loss since the inductor acts as a short circuit and the capacitor acts as an open circuit for such signals. Conversely, a high-frequency signal is blocked by the LPF since the inductor acts as an open circuit and the capacitor acts as a short circuit for such signals.

When a sine wave test signal is passed through an LPF, its amplitude is attenuated as a function of frequency. The relationship between the output and input voltage amplitudes can be expressed as a transfer function. The transfer function,  $V_{out} / V_{in}$ , was measured to determine any effects of the low-residue fluxes.

The transfer function is measured in decibels (dB) as a function of frequency. A decibel can be expressed in terms of voltage as follows:

$$dB = 20 \log_{10} \left| \frac{V_{out}}{V_{in}} \right| \quad (B.9)$$

The PTH transfer function differs from the SMT transfer function due to the self inductance of the capacitor through-hole leads.

### LPF Circuit Board Design

The three LC LPFs for each of the SMT and PTH circuits were designed to have the following cutoff frequencies: 800, 400, and 200 MHz. Cutoff frequency is

that frequency for which the transfer function is -3 dB. The respective component values chosen for the LC filters are 16 nH (nano-Henries) and 6.4 pF (pico-Farads), 32 nH and 13 pF, and 65 nH and 24 pF. Most LPF circuitry was placed on Layer 1, with Layer 2 used as a ground plane. Crossovers needed to connect the LPF circuits are on Layer 4.

The LPF circuits were designed to operate with a 50Ω test system, so all interconnect traces longer than 0.10 inches were designed as 50Ω transmission lines to avoid signal distortion. The LPF circuits were predicted to have less than 2 dB loss below 150 MHz, approximately 6 dB loss near 235 MHz, and greater than 40 dB loss at 550 MHz and beyond. The measured response of the LPF/SMT circuit is close to that predicted except that the transfer function decreases more rapidly than predicted above 350 MHz. As stated previously, the PTH circuit transfer function did not perform similarly to the SMT, particularly at frequencies above 150 MHz.

### TLC Circuit Description

Figure B-3 shows a diagram of the TLC subsection. The LPFs described above are *lumped-element* circuits since the capacitors are discrete components. The TLC lines are *distributed-element* circuits with the resistors, inductors, and capacitors distributed along the lines. A circuit model for the lines is shown in Figure B-4.

The inductance and capacitance for a transmission line with a ground plane are, respectively:

$$L_L = 0.085R_0\sqrt{\epsilon_r}nH / in \quad (B.10)$$

$$C_L = \frac{85}{R_0}\sqrt{\epsilon_r}pF / in \quad (B.11)$$

where  $R_0$  = characteristic resistance and  $\epsilon_r$  = dielectric constant of the board material.

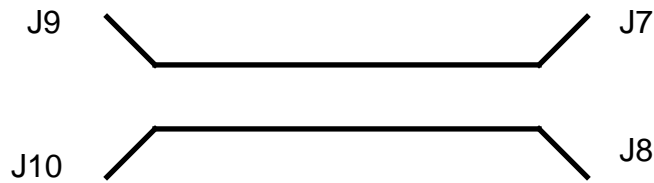
The TLC  $R_0$  was designed to be 50Ω for operation with a 50Ω test system. For FR-4 epoxy (board substrate material),  $L_L$  is about 9.6 nH/in and  $C_L$  is about 3.8 pF/in.

The TLC was tested with a sine wave signal similar to the one used in testing the LPFs.

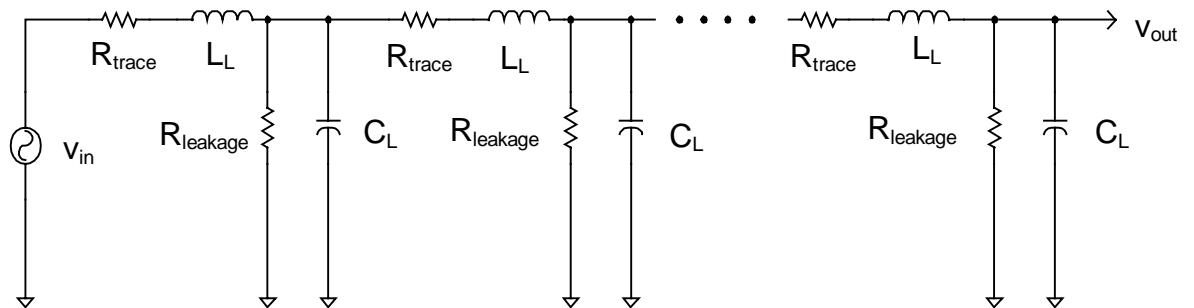
The source resistance was 50Ω and the three output terminals were connected to 50Ω loads.

## TLC Circuit Board Design

The transmission line coupler (TLC) circuit has a pair of coupled  $50\Omega$  transmission lines with required measurable performance frequencies less than 1 GHz. Layer 4 of the printed wiring board (PWB) was used to route the TLC circuit, with Layer 3 used as the ground plane. The TLC circuit is a 5 inches long pair of 0.034 inches wide  $50\Omega$  transmission lines spaced 0.010 inches apart. The circuit design incorporated the board dielectric constant of about 4.8 inches and the .020 inch spacing between copper layers. A computer-aided circuit design tool (Libra) was used to model the TLC circuit. Performance measured on a test PWB agreed very closely with the forward and reverse coupling predictions between 45 MHz and 1 GHz.



**Figure B-3. Diagram of the HF/TLC Subsection**



**Figure B-4. HF/TLC Distributed Element Model**

## **B.6. OTHER NETWORKS (LEAKAGE CURRENTS)**

The LRSTF board also contains three test patterns to provide tests for current leakage: (1) the pin-grid array (PGA), (2) the gull wing (GW), and (3) 10-mil spaced pads. A 5 V source was used to generate leakage currents.

### Purpose of the Experiments

The PGA, GW, and 10-mil pads allow leakage currents to be measured on test patterns that are typical in circuit board layouts. These patterns contain several possible leakage paths and the leakage could increase with the presence of flux residues and environmental exposure. In addition, solder mask was applied to portions of the PGA and GW patterns to evaluate its effect on leakage currents and the formation of solder balls.

### Pin-Grid Array

The PGA hole pattern has four concentric squares that are electrically connected by traces on the top layer of the board as shown in Figure B-5. The pattern also has four vias just inside the corners of the innermost square that are connected to that square. Four vias were placed inside the innermost square to trap flux residues. Two leakage current measurements were made: (1) between the two inner squares (PGA-A) and (2) between the two outer squares (PGA-B), as shown in Figure B-5. Solder mask covers the holes of the two outer squares on the bottom layer, allowing a direct comparison of similar patterns with and without solder mask.

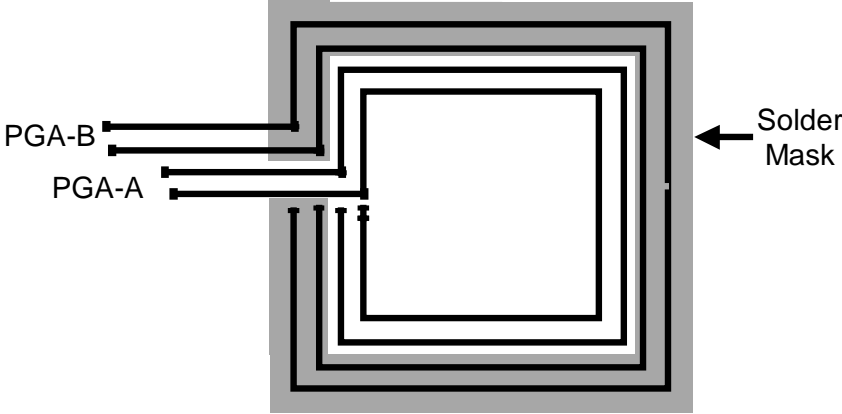
Rather than an actual PGA device, a socket was used since it provided the same soldering connections as a PGA device. Also, obtaining leakage measurements on an actual PGA is nearly impossible due to complexity of its internal semiconductor circuits.

### Gull Wing

The upper half of the topmost GW lands and the lower half of the bottom most GW lands were covered with solder mask to create a region that is susceptible to the formation of solder balls. The lands were visually inspected to detect the presence of solder balls. A nonfunctional GW device is installed with every other lead connected to a circuit board trace forming two parallel paths around the device. Total leakage current measurements were made on adjacent lands of the GW device

### 10-mil Pads

The 10-mil pads were laid out in two rows of five pads each. The pads within each row were connected on the bottom layer of the board and leakage between the rows was measured.



**Figure B-5. PGA Hole Pattern with Solder Mask**

## **B.7. STRANDED WIRES**

Two 22-gauge stranded wires will be hand soldered just to the left of the edge connector. One wire will be soldered directly into the board through holes and the other will be soldered to two terminals, E17 and E18. Each wire is 1.5 inches long, is silver coated, and has white PTFE insulation. All wires will be stripped, tinned, and cleaned in preparation for the soldering process.

### Purpose of the Stranded Wire Experiment

Stranded wires were used to evaluate flux residues and subsequent corrosion.

### Circuit Description

The 5 A 100  $\mu$ s pulse used to test the HCLV circuit was injected into each of the stranded wires for electrical test. A separate PWB trace was connected to each end of the stranded wire. Test wires were connected to the separate traces allowing to provide the means to measure the voltage drop across the stranded wires. In this manner, the voltage drop was measured independently from any voltage drop in the test wires conducting the 5 A pulse to the stranded wires.

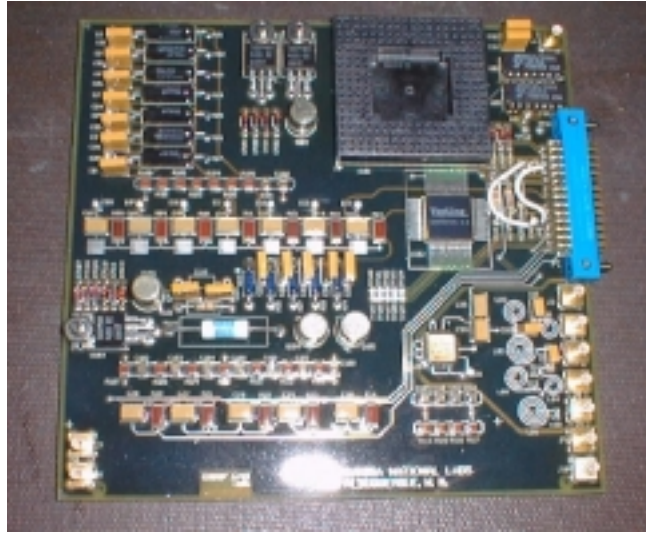
## **B.8. COMPONENTS**

All functional component types conformed to commercial specifications and were ordered pre-tinned (to the extent possible). Components will not pre-cleaned before use.

Solderability testing will be performed using dip and look testing per MIL-STD-202, Method 208 with type R flux per MIL-F-14256. All functional components are required to pass solderability testing.

## B.9. BOARDS

The four-layer LRSTF PWBs have exposed traces on both sides and will be manufactured to meet the requirements of MIL-P-55110. The substrate material will be FR-4 epoxy. Starting copper weight will be 1 oz/ft<sup>2</sup>. An ionic cleanliness level of 5 or less  $\mu\text{g}/\text{in}^2$  NaCl equivalence will be specified.



**Figure B-6. LRSTF Functional Test Board**