



# JG-PP Email

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Joint Group on Pollution  
Prevention

**From:** Brian Greene, Project Integrator  
**Date:** 9/13/02  
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**Pages:**

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## *JG-PP Lead-Free Solder Project Technical Meeting Minutes August 13-14, 2002*

*Govt. Project Manager: Warren Assink, WPAFB*

**Comments:**

Attached please find the minutes from the August 13-14, 2002, 2002, Lead-Free Solder Technical Meeting in Dallas, TX. If you have questions about the minutes, please contact Warren Assink or Brian Greene. Please further distribute as necessary.

**MEMORANDUM FOR RECORD**

**September 9, 2002**

**Subject: Meeting Summary and Minutes – August 13-14, 2002**

**Material(s) Identified:** Lead

**Process Identified:** Electronics soldering

**Methodology Phase:** I-Identification, II - Technical

**Summary:**

On August 13-14, 2002, technical representatives from American Competitiveness Institute, the Boeing Company, ITB, Inc., Lockheed Martin, U.S. Marine Corp., MBDA (U.K.), NASA-Marshall Space Flight Center, Raytheon, Redstone Army Arsenal, Robins Air Force Base, Texas Instruments, Randolph Air Force Base, Rockwell Collins, TRW/ICBM, United Defense Limited Partnership, and Wright Patterson Air Force Base participated in a meeting with representatives from the Joint Group on Pollution Prevention Working Group. The objective of the meeting was to further develop the Joint Test Protocols for Manufacturing and Repair, and discuss the short list of lead-free solder alloys, test board design, and potential testing cost.

During the two-day meeting changes were made, real-time, to electronic copies of the documents that were presented. The revised, updated copies of the documents are included with the minutes as attachments.

**Prior Decisions:**

- 5/9/01 – Lead as used is tin-lead (Sn/Pb) solder was chosen as the target HazMat.



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- 6/20/01 – A Joint Test Protocol (JTP) will be developed for qualifying lead-free solder alloy used in the manufacture of lead-free printed wiring assemblies (PWAs)
- 11/1/01 – A second JTP will be developed for qualifying lead-free solder alloy used in the repair of lead-containing PWAs.
- 3/7/02 – By consensus, the solder alloys currently recommended for testing are:

Wave Solder:	Sn/0.7Cu
	Sn/3.9Ag/0.6Cu
	Sn/3.4Ag/1.0Cu/3.3Bi
Reflow/Manual Solder:	Sn/3.9Ag/0.6Cu
	Sn/3.4Ag/1.0Cu/3.3Bi
Baseline:	Sn/37Pb

**Next Teleconference:** October 1, 2002, 11:00 AM Eastern (tentative)

**Next Meeting:** TBD



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### Minutes

1. Mr. Brian Greene, NASA Acquisition Pollution Prevention Office/ITB, opened the meeting by reviewing the meeting objectives, agenda, and specific discussion topics (see Attachment 2 of minutes). Mr. Warren Assink, Air Force Materiel Command, WPAFB, additionally welcomed everyone to the meeting.

2. **Test Matrix & Test Flow.** Mr. Jeff Bradford, Raytheon, presented some ideas (Test Vehicle Update.ppt) for further streamlining the overall test matrix to achieve the same objectives at less cost. Decisions made by the group were incorporated into the test matrix real-time, allowing the group to see the changes as they are being made. Mr. Bradford began by reviewing which solders and soldering methods were being proposed for both the Manufacturing and Repair testing programs. Manufacturing procedures will include reflow soldering with SnAgCu and SnAgCuBi solder alloys while wave soldering will be done using SnAgCu and SnCu. Repair procedures will be performed using SnPb for reflow and wave solder, SnAgCuBi and SnAgCu for repair soldering of surface mount technology components and SnCu and SnAgCu for repair soldering plated-through-hole components.

3. Mr. Bradford stated that he has a few other ideas that could be incorporated into the test matrix that could reduce the overall cost of the test program. Mr. Bradford will make additions to the test matrix that reflects his ideas (**LFS.02.08.01**).

4. Mr. Tom Woodrow suggested and the group agreed that one test board from each category would be placed in storage and undergoes no testing procedures, as a "standard". This board will be subjected to post test analysis, including cross sectioning to evaluate intermetallic interactions and molecular coarseness, to determine the effects of ambient conditions on the test boards.

5. **Solder Alloys.** Mr. Doug Romm of Texas Instruments raised questions about the wettability of SnCu solder and stated that SnAgCu may be a more suitable solder alloy. It was noted that SnCu was included in the JG-PP solder alloy short list for wave soldering because: NEMI recommended Sn0.7Cu for use by industry as a standardized lead free solder for wave applications, the SnCu alloy system has been previously investigated in a number of wave solder trials by others, and because some military depots are purchasing SnCu alloys off the shelf at local stores. Mr. Romm also questioned contamination issues between Bi and Pb. Mr. Tom Woodrow stated that he is currently conducting tests examining Pb contamination issues and Bi is part of the testing. Mr. Woodrow will share test data with the group when testing is complete. Mr. Mark Strickland commented that he knew of some ongoing studies within NASA that were examining repair work and lead-free solder interaction. Mr. Strickland will compile information on the studies and provide the information to Mr. Greene by September 9, 2002 (Action Item **LFS.02.08.02**).

6. **Joint Test Protocols (Manufacturing & Repair).** Discussion was then directed to extended tests, specifically, which stakeholders require extended testing and which specific test(s) is (are)



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required? The group agreed to add humidity to the extended test matrix; the extended test matrix now includes Temperature-Altitude, Humidity, Rain, Fungus, and Salt Fog testing (a test flow chart appears in attachment Test Vehicle Update.ppt). Stakeholders requiring extended tests need to identify the test and specific parameters and submit the information to Mr. Greene by September 9, 2002 (**Action Item LFS.02.08.03**).

7. The group then discussed the inspection of test boards following testing. It was agreed that the test boards would have to undergo testing at more than one site and that the site doing the testing should also perform the post-test inspection. The group decided that a standardized checklist should be developed for the post-test analysis process (**Action Item LFS.02.08.04**).

8. Mr. Joe Felty stated that a combined environments test would be a very useful tool to include into the test program as a replacement for the HALT Test. An example of a combined environments test would include a temperature cycle, -55°C to +125°C and a vibration spectrum to be run simultaneously. Mr. Hillman stated that Rockwell Collins is starting to incorporate combined environments testing into their testing programs. Mr. Hillman will provide vibration testing information and HALT information from past testing programs (**LFS.02.08.05**).

9. Mr. Lee Whiteman stated that he would be able to provide to Mr. Greene the testing procedures that were used in a previous test program titled EMMA (**LFS.02.08.06**). Information from the EMMA test program will be used as a guide in determining specific testing guidelines such as vibration spectrum.

10. Mr. Dave Locker stated the he would work to identify the number of mechanical shocks needed in order for test boards to satisfy general program requirements. Mr. Greene will work to identify the originator of the initial testing diagrams presently included in the Mechanical Shock section of the JTPs (**LFS.02.08.07**).

11. Mr. Bradford presented a table depicting the estimated number of thermal cycles needed to meet failure criteria and translated that into testing duration in days (Test Vehicle Update.ppt). The group agreed that the thermal cycle test needs to be run until failure criteria is met, but disagreed on the number of cycles it will take to reach failure. In order to avoid unnecessary thermal cycle testing, the group agreed that test boards would be evaluated after 5,000 cycles to determine if the test should continue or be stopped. The decision to continue or stop the test will be based on failure criteria and available funding. Mr. Bradford will update the thermal cycle test duration section of the attachment Test Vehicle Update.ppt (**LFS.02.08.08**).

12. **Test Board Design.** Mr. Dave Hillman presented his latest version of the test board layout. He stated that he needed to finalize the layout to determine the cost of the test boards. The main topic of discussion was part size; number of parts and component finishes. The group reviewed the list of components being placed on the test board. Mr. Bradford suggested that in order to reduce cost, only a few components with lead surface finishes should be placed on the lead-free test boards. The group agreed that the following components will not be placed on the board



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with lead finishes: PLCC, Dpak, TSOP, TQFP, SOIC, CSP, and PDIP. The attached files, D-Component Bill of Materials 8.8.02.xls and D-TestBoardRev2.ppt (components being eliminated from the board are highlighted in yellow) show the agreed upon decisions.

13. Mr. Assink ended day one with some introductory comments about the business phase of the project. OEMs will want to submit a concept paper to their Management Council (**LFS.02.08.09**). Mr. Greene added that he would distribute example concept papers to the OEMs for them to use as a guide (**LFS.02.08.10**). Mr. Assink requested stakeholders to start to involve their business POCs from their respective organization and notify Brian Greene of any business POCs that need to be placed on email distribution (**LFS.02.08.11**). The next phases of the test program will involve multiple business decisions in which the correct POCs will need to be involved. Mr. Assink also requested that participating parties identify their past and future in-kind contributions to the program (**LFS.02.08.12**). Following the submittal of in-kind contributions from the participating members of the testing program, Mr. Greene will distribute expected contributions from stakeholders once the cost estimate is better defined (**LFS.02.08.13**).

14. Day two of the meeting focused on the repair aspect of the testing program. It was decided that only certain components would be repaired on the test boards. These components include BGA, TQFP and SOIC. Only repairing three components will reduce the overall cost of the testing program.

15. The group agreed that all repair procedures must be documented in full. Prior to any decisions being made on who will perform the rework procedures an email will be sent out asking participating parties to define their rework procedures and documentation methods (**LFS.02.08.14**). The group will then decide who best can meet the groups repair needs. The second day's meeting was adjourned at approximately 11:30 a.m.

*SIGNED (Approved by W. Assink 9/12/02)*

Warren Assink  
Govt. Project Manager, WPAFB

Attachments:

1. Action Items
2. Meeting Agenda

**Summary of Lead-Free Solder Action Items**  
**As of 8/14/02**

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**New Action Items**

**LFS.02.08.01**

*Date Due:* **09/16/02**  
*Responsibility:* Raytheon (Jeff Bradford)  
*Required Action:* Develop revised test matrix showing other options to reduce costs  
*Comments:*

**LFS.02.08.02**

*Date Due:* **09/16/02**  
*Responsibility:* NASA MSFC (Mark Strickland)  
*Required Action:* Identify studies (past & present) within NASA dealing with lead-free solder. Provide to B. Greene for distribution.  
*Comments:*

**LFS.02.08.03**

*Date Due:* **09/16/02**  
*Responsibility:* All  
*Required Action:* Determine need for extended tests, and if so, include acceptance criteria  
*Comments:*

**LFS.02.08.04**

*Date Due:* **09/16/02**  
*Responsibility:* All  
*Required Action:* Develop standard PWB inspection list and include in JTPs  
*Comments:*

**LFS.02.08.05**

*Date Due:* **09/16/02**  
*Responsibility:* Rockwell Collins (Dave Hillman)  
*Required Action:* Provide vibration testing information and HALT information from past testing programs.  
*Comments:*

**LFS.02.08.06**

*Date Due:* **09/16/02**  
*Responsibility:* ACI (Lee Whiteman)  
*Required Action:* Provide EMMA test procedures to Brian Greene  
*Comments:*

**LFS.02.08.07**

*Date Due:* **09/16/02**  
*Responsibility:* Army (Dave Locker)  
*Required Action:* Provide reasonable number for mechanical shock. Mr. Greene will also try to identify original diagrams  
*Comments:*

**Summary of Lead-Free Solder Action Items**  
**As of 8/14/02**

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**LFS.02.08.08**

*Date Due:* **09/16/02**  
*Responsibility:* Raytheon (Jeff Bradford)  
*Required Action:* Update test schedule based on revised number of thermal cycles  
*Comments:*

**LFS.02.08.09**

*Date Due:* **10/26/02**  
*Responsibility:* OEMs  
*Required Action:* OEMs submit concept paper  
*Comments:*

**LFS.02.08.10**

*Date Due:* **09/16/02**  
*Responsibility:* ITB, Inc. (Brian Greene)  
*Required Action:* Distribute guideline and examples of DCMA concept paper  
*Comments:*

**LFS.02.08.11**

*Date Due:* **09/16/02**  
*Responsibility:* All  
*Required Action:* Identify business POC, if different from technical POC, to attend business meeting  
*Comments:*

**LFS.02.08.12**

*Date Due:* **09/16/02**  
*Responsibility:* OEMs  
*Required Action:* OEMs identify their past and forecasted in-kind contributions, including labor and other expenses for meetings, JTP development, etc.  
*Comments:*

**LFS.02.08.13**

*Date Due:* **09/30/02**  
*Responsibility:* ITB, Inc. (Brian Greene)  
*Required Action:* Distribute expected contributions from stakeholders once cost estimate is better defined  
*Comments:*

**Summary of Lead-Free Solder Action Items**  
**As of 8/14/02**

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**LFS.02.08.14**

*Date Due:* **09/16/02**  
*Responsibility:* ITB, Inc. (Brian Greene)  
*Required Action:* Send out email requesting technical reps to send in repair work procedures, including documentation  
*Comments:*

**Open Action Items**

**LFS.02.07.02**

*Date Due:* **08/09/02**  
*Responsibility:* Potential testing facilities  
*Required Action:* Complete Lab Survey form  
*Comments:*

**LFS.02.03.01**

*Date Due:* **05/10/02**  
*Responsibility:* Rockwell-Collins (Dave Hillman), F-15 (Mark Stibitz), NASA/ITB (Brian Greene)  
*Required Action:* Dave Hillman work with component suppliers and possibly leverage off the EMMA program work on SnPb (POC: Lee Whiteman) to prepare a component list, with pin counts for each component type listed. Once this is completed, Mr. Hillman should work with Mark Stibitz to determine if hybrids can be added.  
*Comments:* Being updated by Dave Hillman

**Action Items Closed at 13-14 Aug Meeting**

**LFS.02.07.01**

*Date Due:* **08/05/02**  
*Responsibility:* Boeing (Tom Woodrow)  
*Required Action:* Provide references for statistically significant sample sizes and other pertinent testing "rules of thumb".  
*Comments:* 07/22/02 – Boeing's comments emailed to everyone. When interpreting thermal cycling data, one piece of important information is the number of cycles required to reach 63.2% failures (called alpha or the characteristic life). Weibull plots for different component types can be compared to determine which type of solder joints last the longest. To generate useful Weibull plots, you must fail a large percentage of the components, which requires many thermal cycles. IPC-SM-785 has equations for calculating the minimum sample size required for valid Weibull plots. The rule of thumb from this document is "For tests for which the test duration is long enough to allow at least half of

**Summary of Lead-Free Solder Action Items**  
**As of 8/14/02**

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the samples to have failed, a minimum sample size of 32 is recommended.” Shorter test times can be achieved by increasing the sample size and vice versa.

**LFS.02.06.01**

***Date Due:*** 07/10/02

***Responsibility:*** NASA/ITB (Greene)

***Required Action:*** Make correction to the JTPs and redistribute the JTPs to the group.

***Comments:*** Comments continue to be received. Look for revised JTPs to be distributed 1st week of August.

**LFS.02.06.02**

***Date Due:*** 07/10/02

***Responsibility:*** Rockwell-Collins (Dave Hillman), NASA/ITB (Greene)

***Required Action:*** Prepare a bill of materials for the test board and distribute to the group.

***Comments:*** In progress

**August 13-14 Lead-Free Solder Meeting Objectives**

**Solder Alloys**

- Confirm list of potential alternatives for testing.

**Joint Test Protocol (JTP)**

- Agree to the necessary engineering and performance requirements to validate lead-free solder alloys
- Define test procedures and acceptance criteria
- Determine which test requirements are common to all programs and which are needed by fewer than all programs (extended tests).
- Finalize the test vehicle design

**Testing**

- Choose order of test execution and select intermediate decision points.
- Identify testing facilities acceptable to the group

**Business Issues**

- Determine nature and extent of affected program and OEM commitment to fund the testing activities
- Estimate the total cost of the testing activities
- Identify likely source(s) of funding
- Identify possible contract vehicle to fund the test activities

The overall goal of this meeting will be (1) the resolution of the above issues so that the JTP and PAR to be completed very soon and distributed for signature, and (2) to lay the groundwork for a potential business meeting to agree to testing locations, reveal everyone's cost share, and discuss the contract vehicle to be used for the testing activities.

**Agenda**

**Day 1**  
**August 13**

0800 - 0825	Welcome & introductions
0825 - 0940	Solder Alloys
0940 - 1000	Break (20 min.)
1000 - 1140	Joint Test Protocol (JTP)
1140 - 1240	Lunch
1240 - 1350	JTP
1350 - 1400	Break (10 min.)
1400 - 1510	JTP
1510 - 1520	Break (10 min.)
1520 - 1600	JTP
1600 - 1610	Recap

**Day 2**  
**August 14**

0800 - 0940	JTP
0940 - 1000	Break (20 min.)
1000 - 1140	Testing
1140 - 1240	Lunch
1240 - 1330	Testing
1330 - 1350	Business
1350 - 1400	Break (10 min.)
1400 - 1510	Business
1510 - 1520	Break (10 min.)
1520 - 1600	Business
1600 - 1610	Action Items, Next Meeting, & Closing Comments
1610	Adjourn

## Some Specific Discussion Topics

### Solder Alloys

- Which solder alloys will be used for repair?
- Does adding tin lead finish components to our lead-free test vehicles meet our primary mission of demonstrating/validating lead-free soldered circuit card assemblies? Specifically, can we optimize board size (and testing cost) by placing only lead-free components on the lead-free test vehicles and tin lead or lead-free components on the baseline (Sn63) boards?
- What will be the amount of alloys needed, as well as flux type and flux percentage (for wire), container type and size?

### Joint Test Protocol (JTP)

- Who does and does not require HALT testing?
- Define test procedures and acceptance criteria
- What are the rework/repair procedures? (Repair JTP)
- Can we define visual acceptance criteria, JTP Section 2.3.1? Is the IPC standard completed for visual acceptance?
- Should the pre-test inspection be more than a visual inspection and a cross section for documentation purposes? At least one stakeholder requires the PWA's be able to pass all J-STD-001, IPC-A-610, MIL-P-55110, etc. standard tests? For example, if the PWA's can't pass the cleanliness test or the plating adhesion test or the plating thickness requirements inspection or the bond strength test, etc., etc., chances of passing auxiliary testing are reduced. Who else has these same requirements?
- At least one stakeholder requires that three standard tests (moisture and insulation resistance, dielectric withstanding voltage, and thermal stress) be included in the auxiliary testing. Who else requires this?
- Do we need to determine parameters for Electrical Performance Test, JTP Section 3.1.1?
- How many temperature ranges will be used for thermal cycling (2)? What are the temperature ranges (-55° to +125°C and -20° to +80°C)?
- How many cycles will be needed for Thermal Cycle Testing? Thermal Shock Testing?
- Is the temperature range for thermal shock -55°C to +125°C?
- What is the duration of the Mechanical Shock Test?
- Do we need to define parameters for Humidity Testing (MIL-STD-810F, Method 507.4= 60°C and 95% RH with a minimum of five 48-hour cycles)? Would it be better to follow test method IPC-9201 and examine the effects of fluxes and cleaning methods (vs. MIL-STD-810F)? If so, should the test board have a comb pattern or a picklefork pattern underneath a part? Or should this test be deleted entirely
- What parameters will be used for the salt fog test?
- What is the minimum number of samples required for Weibull plots?
- One stakeholder would like to see some tests particularly designed to measure the lead-free alloy's resistance to tin whisker growth. Some suggested tests might be a) compressive stresses such as those introduced by torquing of a nut or screw, b) bending or stretching of the surface after plating, c) scratches or nicks in the plating introduced by handling, d) elevated storage temperatures, etc. Is this something that the JG-PP team should tackle, or are others doing this?

**Testing**

- Per stakeholder suggestion, should we use PLCC-44s and LCC-44s on the test board in lieu of the 20 I/O versions? We would then have a chance to see more LCC failures and compare those to previous studies.
- Is the CLCC lead-free finish (Sn) incorrect? TI will offer SnCu if that stands as the wave solder standard for lead-free. The other component suppliers will need to comment. Jeff Cannis sent an email sometime back asking a group of us if we knew of anyone that did supply a Sn as the lead finish with a negative response.
- Does the group agree with the proposed test flow diagrams?
- Does adding tin lead finish components to our lead-free test vehicles meet our primary mission of demonstrating/validating lead-free soldered circuit card assemblies? Specifically, can we optimize board size (and testing cost) by placing only lead-free components on the lead-free test vehicles and tin lead or lead-free components on the baseline (Sn63) boards?
- How will the resistors and hybrid be monitored (i.e., place the resistors in series as one channel on the event monitor, or monitor with an ohmmeter)? How do you monitor a three lead hybrid?
- Will HALT be performed before individual specification testing or in parallel?
- How many boards will get reworked with each solder?
- Based on the responses to the Lab Survey Form, which possible testing facilities seem most acceptable to the group?

**Business Issues**

- Initiate discussion about industry in-kind contributions.
- What is the total maximum cost of the testing and the likely cost of testing (after free services are subtracted)?
- What are the likely source(s) of funding?
- What contract vehicle should be pursued?