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Joint Group on Pollution
Prevention

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***JG-PP Lead-Free Solder Project
Technical Meeting Minutes
November 14-15, 2001***

JG-PP Project Lead: Robert Hill, NASA KSC

Comments:

Attached please find the minutes from the November 14-15, 2001, Lead-Free Solder Technical Meeting in Dallas, TX. If you have questions about the minutes please contact Robert Hill, Brian Greene or Tess Flynn. Please further distribute as necessary.

MEMORANDUM FOR RECORD

November 30, 2001

Subject: Meeting Summary and Minutes – November 14-15, 2001

Material(s) Identified: Lead

Process Identified: Electronics soldering

Methodology Phase: I-Identification, II - Technical

Summary:

On November 14-15, 2001, technical representatives from the Boeing Company, F-15 Program/Robins Air Force Base, Lockheed Martin, Mitsui Comtek/Senju Metals Co., National Aeronautics and Space Administration (NASA)-Kennedy Space Center, NASA-Marshall Space Flight Center, National Center for Manufacturing Sciences, Raytheon, Rockwell-Collins, Texas Instruments, TRW, U.S. Army Missile Command, and U.S. Army Tank-Automotive and Armaments Command participated in a meeting at the Raytheon facilities in Dallas, Texas, with representatives from the Joint Group on Pollution Prevention Working Group and JG-PP contractors. The objective of the two-day meeting was to further develop the circuit card manufacturing Joint Test Protocol for lead-free solders, begin discussing the repair JTP, discuss the test board design, and further refine the list of candidate lead-free solders.

Prior Decisions:

- 5/9/01 - Lead as used is tin-lead (Sn/Pb) solder was chosen as the target HazMat.
- 6/20/01 – A Joint Test Protocol (JTP) will be developed for qualifying lead-free solder alloy used in the manufacture of lead-free printed wiring assemblies (PWAs)

Robert P. Hill, JASPPA Chairman, NASA KSC, 321-867-8466



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- 11/1/01 – A second JTP will be developed for qualifying lead-free solder alloy used in the repair of lead-containing PWAs.

Next Teleconference: December 17, 2001, 11:00 A.M. Eastern time

Next Meeting: TBD

Minutes

1. Mr. Brian Greene, National Aeronautics and Space Administration/International Trade Bridge, Inc. (NASA/ITB) and Project Integrator for the Lead-Free Solder JG-PP project, welcomed everyone to the meeting on behalf of Mr. Robert Hill, who could not attend the meeting. Mr. Greene stressed the importance and urgency of continuing to work on developing a test protocol for lead free solders. It was noted that industry is currently building lead-free assemblies and are ready for full-scale production. There is an increasing desire to get the military to get up to speed with qualifying lead-free solders.
2. Following the welcome, Mr. Joe Felty, Raytheon, discussed the logistics of the meeting. This was followed by each of the participants introducing themselves. The combined participants represented several original equipment manufacturers (OEMs), Army, Marine Corps, Air Force, and NASA.
3. Mr. Greene reviewed the JG-PP methodology and the major documents developed for a typical JG-PP project: the Joint Test Protocol (JTP), Potential Alternatives Report (PAR), Cost Benefit Analysis (CBA), and Joint Test Report (JTR). He explained that the primary focus of the face-to-face meeting was to develop the test protocol details, and the methodology for downselecting lead-free solder alloys. He also stated that Concurrent Technologies Corporation (CTC) had been directed by the JG-PP Working Group to perform a CBA, and that CTC would be seeking input from project representatives interested in providing the nature and extent of their facility's lead solder usage. He explained that this meeting was to be a working meeting, with the group reviewing technical documents, specifications, and existing test data. Mr. Greene acknowledged that a couple of project participants have voiced concern at prior meetings about whether lead-free solder alloys exist that will likely perform well under all environments, including repair. But Mr. Greene asked that, for today's meeting, participants stay focused on developing stand-alone JTPs—one for manufacturing and one for repair processes—that contains the critical performance requirements that a lead-free solder now or in the future must meet. In tomorrow's meeting, the group would discuss the potential lead-free solders for testing, with the goal being to ideally downselect to a handful of solders.
4. Mr. Greene explained that at the November 1 teleconference, the participants decided that two JTPs would be developed—one for manufacturing and one for repair processes. The requirements in these JTPs would be further subdivided into board and component-level requirements. He added that other kinds of testing besides performance testing may be deemed necessary by the



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group, such as screening tests to downselect alternatives and fill in data gaps, and environmental, health and safety tests (e.g., leachability).

5. A question was asked about how can we possibly include everyone's performance requirements in the JTP and everyone's desired components on the test board unless we have every weapon system manager represented at these meetings. Mr. Greene replied that in the past (JG-PP CCAMTF project), it was known that we may only be capturing 80 percent of the requirements of all potentially affected programs, and that each program manager had the final say as to what additional testing their system would require and whether to implement a qualified alternative.
6. **Manufacturing JTP.** The meeting participants pulled out their copies of the current JTP, dated September 18, 2001 and posted on the JG-PP Web site, and began reviewing the key technical sections (Sections 2 and 3). It was noted that this JTP, as written, applies to qualifying solder alternatives for use in manufacturing at the board level. The participants discussed and agreed to the following changes to Section 2, Engineering and Testing Requirements, of the Manufacturing JTP.
 - a. General comments to Manufacturing JTP Section 2:
 - 1) The prior CCAMTF Test set must be redesigned to be applicable for the Lead-Free Solder project. The board to be used for this project must reflect the needs of the group, such as newer test board patterns.
 - 2) Board Level Mfg. The manufacturers of the board materials to be tested must supply their materials to meet the specifications identified by the group. MIL-PRF-55110 (equivalent is IPC 6011 and IPC 6012A) will be the basis for board manufacturer performance and qualification requirements. The JTP should specify our desired reliability requirements that the boards, components, flux and solder alloys must meet.
 - 3) Even though test board requirements will be specified to the manufacturers in the JTP, we must still inspect the assemblies before testing and pre-determine the criteria for which a solder joint is deemed suitable for testing. Visual inspection and photographic documentation will be conducted prior to testing procedures to insure quality. Mr. Bob Vanderwiel, Lockheed Martin, thought that J-STD-001 specifies solder joint requirements, including appearance, for both lead and lead-free solders. Several others took exception, stating that J-STD-001C (which is the latest version) only applies to lead solders, and that there is no published standard specifying the requirements for lead-free solders.
 - 4) Component Level Mfg. The manufacturers of the components for the PWBs must supply their components to meet the specifications identified by the group. MIL-STD-883 will be the basis for component (microelectronic devices) manufacturer performance and test requirements. The JTP should specify our desired reliability requirements that the components must meet. However, there will be no performance testing of the components in the Manufacturing JTP. We will only look at the integrity of the finishes.
 - b. Specific changes to Manufacturing JTP Section 2:
 - 1) Per a comment from Mark Stibitz, Robins AFB/Raytheon, note as a definition that "rework" is a part of the manufacturing JTP. "Repair" processes are entirely different



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from both manufacturing and rework, and will be the subject of a second JTP. The Manufacturing JTP should include a concise definition of what we mean by “manufacturing.”

- 2) Include the requirements of MIL-P-55110 in terms of requirements that board manufacturers must meet.
 - 3) Retitle Table 2 as Common Tests—tests that all of the OEMs and program managers agree are necessary to qualify a lead-free solder.
 - 4) Add a new Table 3 titled Extended Tests—those tests required by one or more programs but not by everyone.
 - 5) A general caveat needs to be stated that if at the conclusion of a particular test no solders (including the lead solder control) have failed, we will run the test at accelerated conditions (e.g., longer cycle times, different vibration profile) to discern any differences in the performance of the alloys.
 - 6) State that the amount of each solder alloy applied to a joint will be the same. For example, the amount of lead solder (in the control) will be the same amount as for the lead-free solders.
7. The meeting participants then reviewed and agreed to the following changes to Section 3, Test Descriptions, of the September 18 Manufacturing JTP.
- a. General comments to JTP Section 3:
 - 1) For all tests, propose to test five board assemblies containing each solder alloy. However, Mr. Felty took an action item (AI) to ask a statistician whether five PWAs was a statistically sufficient number of samples (**AI LFS.01.11.04**), as well as what should be the general criteria for failure (e.g., 2 out of 5; 3 out of 5) (**AI LFS.01.11.05**).
 - 2) 63% tin (Sn)/37% lead (Pb) solder will be the control solder alloy. Unless otherwise specified in this Manufacturing JTP, the acceptance criteria for each test is performance equal to or better than tin-lead solder. The reason: meeting participants felt that performance equal to or better than the control would demonstrate that switching to lead-free solder would not degrade the weapon system performance (understanding that individual program managers may have additional requirements that may need to be met).
 - b. Vibration Test
 - 1) General comments, Vibration Test:

We should test the worst-case vibration scenario. For now, assume missile systems will be the worst case, and use those test specifications as a model for determining the test parameters to use in the JTP. Mr. Keith DeGroot, U.S. Army TACOM, and Mr. Felty agreed to contact their respective organizations to obtain worst-case vibration spectra for inclusion in the JTP Vibration Test (**AI LFS.01.11.06**).
 - 2) Specific Manufacturing JTP changes, Vibration Test:

Under “Rationale”, state “every assembly sees some level of vibration. To cover all vibration spectra, the stakeholders chose the worst-case situation to test.” (Note, this selection still needs to be done.)



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c. Mechanical Shock Test

1) General comments, Mechanical Shock Test:

For now, use the mechanical shock profile provided by the Navy (Mr. John Nelson, China Lake).

2) Specific Manufacturing JTP changes, Mechanical Shock Test:

- a) Under “Rationale”, state that every assembly sees some level of mechanical shock. To cover all shock profiles, the stakeholders chose the worst-case situation to test.
- b) Mr. Greene will contact Mr. Nelson to discern the details of this test as it relates to the shock profile provided by Mr. Nelson, and determine whether the Navy’s shock profile is suitable (or too harsh) for testing (**AI LFS.01.11.07**).

d. Thermal Shock Test

1) General comments, Thermal Shock Test:

- a) MIL-STD-810 and MIL-STD 202 Method 107 traditionally specify the requirements for thermal shock. MIL-STD-202 is for qualifying an assembly (board level). MIL-STD-883 would be for component testing.
- b) Per the military standard, 100 cycles will be the evaluation point. However, we will run the test to 200 cycles or until we can differentiate performance between the various lead-free solders and lead solder control.

2) Specific Manufacturing JTP changes, Thermal Shock Test:

- a) Under “Rationale”, state that “every assembly sees various temperature ranges when in use, and the thermal shock test measures this. The basis for the thermal shock test parameters is MIL-STD 202 Method 107. The temperature range encompasses all the stakeholders’ conditions” (except perhaps for NASA—this needs to be verified).
- b) Per the military standard, 100 cycles will be the evaluation point. However, we will run the test to 200 cycles (or longer) as a “safety factor” to ensure that we can differentiate performance between the various lead-free solders and the lead solder control. Technical representatives should check with respective organizations to make sure that 200 cycles is a sufficient maximum number of cycles to run Thermal Shock (**AI LFS.01.11.08**).
- c) The test parameters are:
 - i) Temperature range of -55°C to 125°C
 - ii) Evaluation points at 100 cycles and 200 cycles as a minimum
 - iii) Transfer rate of 5 minutes maximum from -55°C to 125°C
 - iv) Dwell time of 15 minutes at temperature extremes

e. Humidity Test

1) General comments, Humidity Test:

MIL-STD-810 Method 507.4 traditionally specifies the requirements for humidity testing.

2) Specific Manufacturing JTP changes, Humidity Test:

- a) Under “Rationale”, state that the purpose of this method is to determine the resistance of material to the effects of a warm, humid atmosphere. This is a general corrosion



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test, to see how two different metals interact. All aspects of board assembly are tested with in this test.

- b) The test parameters are:
 - i) 23°C, 50% relative humidity at 24 hours, followed by 30°C, 95% relative humidity at 24 hours = one cycle
 - ii) minimum of 5 cycles of 48 hours each (= 10 day minimum testing)

8. **Repair JTP.** Mr. Greene had not prepared a strawman Repair JTP yet. As an alternative basis from which to discuss requirements for the Repair JTP, copies of a requirements matrix for PWB repair, prepared by Mr. Stibitz for the F-15 program on November 12, 2001, were distributed and reviewed by the meeting participants (see Attachment 1). Mr. Stibitz indicated that MIL-STD-883 was the basis for the following component-level tests suggested for the Repair JTP:

- Lead Finish Adhesion
- Lead Integrity
- Salt Atmosphere
- Lead Finish Thickness
- Solderability
- Thermal Shock and Temperature Cycling
- Solvents
- Moisture
- Mechanical Shock and Constant Acceleration
- Seal, Fine Leak, & Gross Leak
- Burn-in
- Electrical Performance, Pre/Post Burn-in
- Steady State Life
- Internal Visual Inspection
- SEM Inspection

9. The group discussed a number of issues related to component-level repair and agreed upon the following:

- a. The manufacturers of the components for the PWBs must supply their components to meet the specifications identified by the group. MIL-STD-883 will be the basis for component manufacturer specifications, along with any other specifications identified by the project stakeholders. The JTP should specify our desired reliability requirements that the components must meet. However, there will be no performance testing of the components in the Manufacturing JTP. We will only look at the integrity of the lead finishes and soldered interconnects.
- b. The main issue with repair is the intermetallic interactions that occur between new alloy and lead solder already on the PWB.
- c. Just as with the Manufacturing JTP, the Repair JTP should include a concise definition of what we mean by “repair.”
- d. MIL-STD-883 will probably be the primary standard serving as a basis for the tests in the Repair JTP (at least the F-15 Program agrees), but other possible standards include J-STD-001, 002, & 003, and MIL-PRF-38534 and 38535.
- e. The F-15 program is very much interested in the repair of hybrid boards (application-specific circuits). An area of concern for hybrids is tin whiskers. Mr. Dave Hillman, Rockwell-Collins, indicated that he has data that he will share with the group describing the method by



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which tin whiskers form (**AI LFS.01.11.09**). This could be used to eventually develop a means of controlling tin whiskers.

- f. Mr. Stibitz indicated that he did not see the value of including burn-in, even though MIL-STD-883 mentions it. Burn-in only addresses component (microelectronic device) manufacturing defects, and would not help discriminate between solders.
- g. Visual testing—Wetting angle and geometry is the key to proper joint integrity, not visual appearance. For these reasons, the IPC, over the next two years, will be developing new specifications for no-lead solder joints to address their differing visual appearance compared to conventional lead solder joints.
- h. Lead contamination issue. Cycling tests to the point of component interconnect failure is recommended to discern lead contamination.
- i. Mr. Greene will incorporate all these comments into a strawman JTP, which he will then distribute for review and comment (**AI LFS.01.11.10**).

- 10. Mr. Tom Woodrow, Boeing, brought up the possibility of testing that may be necessary to answer the lead contamination issue brought up at prior meetings. One possibility is to contaminate the lead-free solder joints with known amounts of lead and look for joint failure. Such testing would also help answer whether the presence of bismuth in lead-free solder affects the joint reliability. All agreed that such testing would fall into the category of “data gap” testing and would not necessarily be part of the Repair JTP. It would also probably involve using a separate test vehicle.
- 11. The following table summarizes the applicability of military standards to the two JTPs.

Solder Application	Board/Assembly Level (external to components)	Component (Microelectronic Device) Level
PWB Manufacturing	<p style="text-align: center;"><i>Mfg. JTP</i></p> <p><u>MIL-STD-202</u></p> <p>Include requirements that board mfrs. must meet into <i>Mfg. JTP</i></p> <p>Test and evaluate the <u>performance</u> of the solders per the tests in the <i>Mfg. JTP</i> (9/18/01)</p>	<p style="text-align: center;"><i>Mfg. JTP</i></p> <p><u>MIL-STD-883</u></p> <p>Include requirements that component mfrs. must meet into <i>Mfg. JTP</i></p> <p>Examine only the <u>integrity</u> of the lead finishes and soldered interconnects; No specific JTP component testing.</p>
PWB Repair	<p style="text-align: center;"><i>Mfg. JTP</i></p> <p><u>MIL-STD-202</u></p> <p>Defined as “rework”, therefore same requirements as above for</p>	<p style="text-align: center;"><i>Repair JTP</i></p> <p><u>MIL-STD-883</u></p> <p>Develop a <i>Repair JTP</i> for component testing</p>



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	<i>Mfg. JTP, Board Level</i>	
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12. **Test Board Design.** Mr. Felty and Mr. Jeff Bradford presented the test board design for the Manufacturing JTP that they proposed a couple of months ago for the project. They compared the proposed test board to the existing Low-Residue Soldering Task Force (LRSTF) test board.
- a. After some discussion, the group reached consensus on the following design considerations for the test board for the Manufacturing JTP:
- 1) 20 Pin Leadless Chip Carrier to replace 44 pin LCC
 - 2) No TLC and LPF—this is old technology and low frequency
 - 3) No dummy components, therefore visual inspection for solder joint cracks is not required
 - 4) No stranded wire, since experience is these don't fail much
 - 5) Need PTH and SMT components. PTH because it will allow for intermetallic failure to be discerned and because Army still uses a lot of it.
 - 6) No ICs, or at least significantly limit the number of complicated, active ICs. Instead, we will just put on a very few simple active electrical circuits to allow for discernment of lead vs. lead-free solders. Also, we will require the manufacturer to meet MIL-STD-883.
 - 7) Add both ceramic and plastic BGA, since newer components
 - 8) No Flip Chips—these will not be used much in the future
 - 9) Add 0.8mm Chip Scale Package (CSP), D-Pack, and pin grid array. Mr. Hillman will look into the possibility of having a vendor supply defective capacitors that are shorted (**AI LFS.01.11.11**).
 - 10) Boards will be made of high-temperature, $T_g=170\text{ }^\circ\text{C}$ (polyimide) laminate for new manufacturing. Industry is moving in the direction of using these board types by 2006.
 - 11) Board surface finish will be immersion silver. Immersion silver is more robust and offers better temperature resistance (it can be heated and reheated several times). Mr. Woodrow has data from Lucent Technologies on immersion silver that he will provide to everyone (**AI LFS.01.11.12**). Just to be sure that immersion silver does not adversely affect lead-free solder performance, we will run one set of thermal cycling tests with an organic solderability preservative (OSP) surface finish, such as benzimidazole, so that we have a few data points to compare the effect of surface finish (none is anticipated). Surface finishes will be applied in two passes: first pass for PTH, second pass for SMT.
 - 12) Flux: Manufacturers of the selected solder alloys will select the best flux for their product.
 - 13) Cleanliness: Regardless of the flux, all boards must be totally clean prior to testing. We will measure cleanliness before testing, as well as ask the vendor to verify that all residues will be removed.
 - 14) No decision was made on whether to include flex boards. Ms. Martha Schuster, Redstone Army Arsenal, agreed to check the extent to which components are being soldered to flex boards in Army missiles and aviation (**AI LFS.01.11.13**).



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The changes noted above represent a significant deviation from the CCAMTF test board, but are deemed necessary to have a board that is representative of today's conditions. Mr. Felty, Mr. Bradford, and Mr. Hillman agreed to prepare a list of the microelectronic devices proposed for the test board and the cost and availability (**AI LFS.01.11.14**). The desire is to see if all the components will fit on one board for a reasonable price.

- b. A number of decisions were made concerning the design considerations for the test board for the Repair JTP. As a start, we will include the same requirements and components as for the Manufacturing JTP, except as noted below
 - 1) Include stranded wire, since this is commonly found on boards that are repaired.
 - 2) Boards to be made of low-temperature, $T_g=125\text{ }^\circ\text{C}$ (glass epoxy) laminate for repair work—these board types are already in use. However, Mr. Stibitz agreed to survey within Robins AFB to ascertain the percentage of solders that are high-temperature vs. low-temperature (**AI LFS.01.11.15**). If one of the other of these laminates is a very low percentage, there would not be great value in testing it.
 - 3) Board surface will be tin-lead so that there is a possibility of causing an intermetallic effect, which we will then measure the effects of.

13. **Other Issues**. Several other issues were discussed pertaining to the technical phase of the project.

- a. There will likely be a need for a professional statistician for statistical inference of data gathered from testing. Mr. Felty will look into this.
- b. Communication and Marketing. Mr. Greene will talk to Mr. Bob Hill about developing a position/ rationale paper to be given to the program managers describing the arguments for going ahead with the no-lead solder project, such as:
 - 1) Parts obsolescence, suppliers going to no-lead
 - 2) Need articles that express the manufacturers shift to no-lead solder
 - 3) DLA can only stockpile parts for 2 years by law

14. The second day of meetings began with a review of the day's objectives by Mr. Greene and a summary of the purpose of two of the other JG-PP documents—the Potential Alternatives Report (PAR) and the Cost Benefit Analysis (CBA). Next, Mr. Bradford displayed the following chart summarizing the decisions made at the first day's meeting concerning the solders and coatings that will be applied to the test board. The group agreed that the matrix correctly reflected the decisions made.

Type of Application	Laminate	Surface Finish	Solder Alloy	Repair Solder
Mfg.	Hi temp	Immersion silver	Lead-free (abt. 3)	N/A
Mfg. Control	Hi temp	Tin-lead by hot air solder leveling (Sn-Pb HASL)	63Sn/37Pb	N/A
Repair	Low temp	Sn-Pb HASL	63Sn/37Pb	Lead-free (1)
Repair Control	Low temp	Sn-Pb HASL	63Sn/37Pb	63Sn/37Pb



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15. Mr. Marv Bellamy, Senior Reliability Engineer at Raytheon, next presented information about the Highly Accelerated Life (HALT) test procedure. HALT was designed as a method for quickly detecting design and manufacturing defects in PWAs. It tests the PWAs at predetermined environmental extremes. The movement to those extremes occurs very rapidly (within minutes). The procedure requires a special HALT chamber, which Raytheon has. The tests are run to failure. Mr. Bellamy thought HALT would be very well suited to discerning differences among different solder alloys. Mr. Stibitz suggested to the group that HALT be included in the repair JTP. He thought the harshest vibration environment would be on aircraft during gunfire, and that HALT would be a good determining test of the strength of the repaired solder joint under such a severe environment.
16. Mr. Ron Patun, NDCEE/CTC, delivered a briefing on the progress CTC has made on the PAR and initial CBA. Mr. Patun also distributed three different CBA survey forms that CTC planned to use in the near future to solicit feedback from OEMs and repair facilities on the nature and extent of their lead soldering activities. The information from these baseline surveys will be used to compare the lead-free solders to. One specific comment to Mr. Patun was that maintenance and decommissioning activities need to be incorporated into the solder survey forms. An action item was taken for everyone to provide comments on suggested improvements to the CBA forms to Mr. Patun as soon as possible (**AI LFS.01.11.16**). Mr. Hillman and Mr. Felty indicated that Rockwell-Collins and Raytheon would likely be interested in completing a CBA survey form for PWA manufacturing. An action item was taken for everyone who might be interested in completing a CBA survey form, to provide a point of contact to Mr. Patun (**AI LFS.01.11.17**).
17. On the subject of potential alternatives, Mr. Patun presented a summary matrix of performance, cost, and toxicity information published on a variety of lead-free solder alloys, as well as some papers summarizing NCMS's lead-free solder test data. Mr. Woodrow noted some confusion about what upper temperature limit the lead-free solders were tested to in the NCMS study, and therefore what temperature ranges lead-free solders seem best suited. Mr. Napp replied that, based on NCMS thermal cycling testing (from -40 to 125 °C) of plastic ball grid arrays, lead-free solders perform *better* than conventional tin-lead solders in this "lower" temperature range (less than 125 °C).
18. Next, Mr. Derek Daily, Mitsui Comtek/Senju Metals Co., presented test data and other technical information that he has collected from their customers on lead-free solder performance. According to Mr. Daily, Senju is the world's second largest solder manufacturer. Senju also provides complete lead-free systems, such as ovens to allow temperature profiles to be met. Mr. Daily's technical information is on CD and is available to anyone who asks. The information on the CD is organized into four "bulletins". Of interest to this project, Bulletin 2 contains information that Senju used to downselect to six lead-free solder alloys and three different flux chemistries. Bulletin 3 may be of most interest to this project because it offers direct comparison between lead and lead-free solders, including performance on additional circuit card components (e.g., BGA and daisy chain). Among the conclusions offered by Mr. Daily include the following:



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- The overall process (type of flux and PWB surface finish) is important in determining solder performance.
- The type of surface finish is often the initial mode of failure. Immersion silver is a very good surface finish to use with lead-free solder, whereas a thick gold finish is not good to use.
- Using a lead-free solder with a lead-free process actually offers better performance than a lead solder with a lead process. Lead-free PWBs tends to exhibit fewer failures with increase in cycle times.

Aside from these variables, Mr. Daily noted some general trends in solders being tested and recommended by other groups (e.g., NEMI, Japan's JATA):

- The tin-silver-copper solder alloys, where silver is in the 3.5-4.0% range and copper in the 0.5-0.75% range, are most often being recommended. (Japan is starting to move away from the tin-silver-copper-bismuth alloys to tin-silver-copper because of the ease in working with it due to its enhanced wettability.)
- Tin-3.5silver is also popular (especially with automotive industry) and has been around for a while.
- Bismuth-containing solders tend to exhibit fillet lifting. The automotive industry uses bismuth solders, but not for plated through-hole.

Senju's Web site is <http://www.senju-m.co.jp/e/index.htm>.

19. Mr. Leake asked whether it was wise to let the solder suppliers specify the flux, or whether we should select it ourselves. After some discussion, the consensus of the group was that we should let the solder alloy supplier recommend the flux based on the performance requirements that we stipulate.
20. Cleaning of the PWBs was also discussed. Senju's CD contains information on cleaning products. Mr. Mike Bixon at Kysen is a recommended POC for obtaining information on cleaning lead-free assemblies. Zeston (Germany) is another good cleaning company.
21. Next, Mr. Felty presented the his own short list of lead-free solder alloys, which was based on his review of work conducted by Ms. Jennie Hwang (SMT/July 2001) and others. After some discussion by the group, Mr. Felty's list was modified as follows.

Baseline Solder

- 63Sn/37Pb

Wave Solder

- Sn/0.7Cu (NEMI)
- **Sn/3.9Ag/0.6Cu (NEMI)** (added, based on prior favorable performance, and so that we have at least one solder tested in two programs)

Reflow/Manual Solder

- Sn/3.9Ag/0.6Cu (NEMI)
- ~~Sn/3.4Ag/4.8Bi (further restudy—NCMS)~~ (delete—Bi content is too high—it may form a eutectic with lead solder contaminants; also, manufacture of raw Bi

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generates a lot of Pb slag, which is environmentally undesirable. Ideally want around 3.0% Bi or less.)

- Sn/3.1Ag/0.5Cu/3.1Bi (H – Technologies)

21. The group discussed who will be providing the various materials for testing. Mr. Doug Romm, Texas Instruments, indicated that TI was still willing to supply components. Mr. Daily indicated that Senju would be willing to supply the solders and fluxes. A group member thought that the American Competitiveness Institute had a small wave solder machine. Mr. Woodrow indicated that Boeing-Seattle had plans to install a 700-lb. wave solder pot dedicated to lead-free solder for surface mount technology and plated through-hole. Mr. Daily was subsequently asked if he knew whether Sn/Ag/Cu and Sn/Ag/Cu/Bi solder alloys had been applied using wave solder. Mr. Daily thought they had been, but agreed to confirm with Senju's customers (**AI LFS.01.11.18**).
22. Mr. Greene was assigned an action item to schedule a mid-December teleconference to discuss lead-free solder alternatives, the two JTPs, and the continuing work on test board design (**AI LFS.01.11.19**).
23. Mr. Greene reviewed the two days' action items. He then thanked the participants for their constructive participation over the past two days. He especially thanked Raytheon for hosting the meeting. The meeting was adjourned at approximately 11:30 a.m.

SIGNED (Approved by B. Greene for R. Hill 11/30/01)

Robert P. Hill
JASPPA Chairman, NASA KSC

Attachments:

1. MIL-STD-883 Critical Performance Requirements for PWB Repair, per F-15 Program
2. Action Items

Lead-Free Electronics Soldering COMPONENT LEVEL Performance Requirements				
A. Test Requirement	B. Test Method (plus any unique criteria?)	C. Basis for Requirement	D. Programs Requiring Test	E. Additional Comments on Test Procedure
Thermal Shock or Temperature Cycling	MIL-STD-883, TM 1011 or TM 1010	Verify lead solder joint integrity. Temperature cycling identifies failures that Thermal Shock cannot. MIL-M-38510, MIL-PRF-38534, MIL-PRF-38535, Applicable OEM Specifications	F-15	5 pieces Cond A, Min. 5 pieces Cond C, 1000 cycles
Solvents	MIL-STD-883, TM 2015	Verify lead solder finish integrity, susceptibility to cause corrosion. MIL-M-38510, MIL-PRF-38534, MIL-PRF-38535, Applicable OEM Specifications	F-15	3 pieces
Moisture	MIL-STD-883, TM 1004 or TM 1018	Verify lead solder finish integrity. MIL-M-38510, MIL-PRF-38534, MIL-PRF-38535, Applicable OEM Specifications	F-15	5 pieces
Mechanical Shock or Constant Acceleration	MIL-STD-883, TM 2001 and/or TM 2002	Verify lead solder finish integrity. Constant Acceleration will identify failures that Mechanical Shock cannot. MIL-M-38510, MIL-PRF-38534, MIL-PRF-38535, Applicable OEM Specifications	F-15	5 pieces, Cond B, Y1 Direction 5 pieces, Cond B, Y1 Direction

Lead-Free Electronics Soldering COMPONENT LEVEL Performance Requirements				
A. Test Requirement	B. Test Method (plus any unique criteria?)	C. Basis for Requirement	D. Programs Requiring Test	E. Additional Comments on Test Procedure
Seal Fine Leak Gross Leak	MIL-STD-883, TM 1014	Verify package seal MIL-M-38510, MIL-PRF-38534, MIL-PRF-38535, Applicable OEM Specifications	F-15	15 pieces, Cond A or B 15 pieces, Cond C or D
Burn-in	MIL-STD-883, TM 1015	MIL-M-38510, MIL-PRF-38534, MIL-PRF-38535, Applicable OEM Specifications	F-15	
Electrical Performance, Pre/Post Burn-In	MIL-STD-883, TM 5004 and TM 5005	Verify solder signal carrying capability, signal loss. MIL-M-38510, MIL-PRF-38534, MIL-PRF-38535, Applicable OEM Specifications	F-15	Would be tough to pin down. Would have to identify OEM requirements for specific part type used.
Steady State Life	MIL-STD-883, TM 1005	Verify electrical performance and life of solder over time	F-15	20 pieces, 1000 hours @ 125 deg. C
Internal Visual Inspection	MIL-STD-883, TM 2017 (hybrid), TM 2013 (DPA), and TM 2014 (Internal Visual & Mechanical)	Verify lead solder finish integrity, susceptibility to cause corrosion	F-15	
SEM Inspection	TBD	Verify metallization	F-15	

NOTE: MIL-M-38510 is inactive for new designs, but is still applicable due to the need to support existing older technologies used in the F-15.

ADDITIONAL QUESTIONS (please answer)

1. Does the following describe an adequate baseline for testing?

- Baseline solder: eutectic (63/37) (medium temperature) solder alloy
- Board finish: Sn-Pb and Hot Air Level Soldering (HASL)
- Board (laminated) type: FR-4
- Components: mix of finish leads
- Component configurations: mixed, TH & SMT board components, & connectors (with and without different [gold] finishes)
- Surface finish: Sn-Pb and lead-free
- Process application technology: wave, reflow, manual, and heat shrink
- End-item performance environment: wide range: controlled to harsh
- Flux type: as recommended by solder manufacturers (get data to narrow down)

_____ No Please explain _____

Should we be concerned with solder performance under conformal coating? Two main types: Polyurethane and parylene.

2. What is the highest temperature (deg. F) that your existing hardware to be soldered can withstand?

Component after manufacture: -55 deg. C (-67 deg. F) to + 125 deg. C (+257 deg. F).

Local point to be soldered (typical temperature before eyelet is lifted off PWB): 350 deg. C (665 deg. F) to 450 deg. C (850 deg. F).

New Action Items

LFS.01.11.04

Date Due: 12/11/01

Responsibility: Raytheon (Joe Felty)

Required Action: JTPs. Ask a statistician whether five PWAs was a statistically sufficient number of samples.

Comments:

LFS.01.11.05

Date Due: 12/11/01

Responsibility: Raytheon (Joe Felty)

Required Action: JTPs. Ask a statistician what should be the general criteria for test failure (e.g., 2 out of 5; 3 out of 5)

Comments:

LFS.01.11.06

Date Due: 12/11/01

Responsibility: Army (Keith DeGroot), Raytheon (Joe Felty)

Required Action: Manufacturing JTP. Contact their respective organizations to obtain worst-case vibration spectra for inclusion in the Manufacturing JTP Vibration Test.

Comments:

LFS.01.11.07

Date Due: 12/04/01

Responsibility: NASA/ITB (Brian Greene)

Required Action: Manufacturing JTP. Contact John Nelson, China Lake, to obtain details of the shock profile provided earlier by Mr. Nelson and determine its suitability for inclusion in the Manufacturing JTP Mechanical Shock Test

Comments:

LFS.01.11.08

Date Due: 12/11/01

Responsibility: All technical representatives

Required Action: Manufacturing JTP. Check with respective organizations to make sure that 200 cycles is a sufficient maximum number of cycles to run Thermal Shock for the Manufacturing JTP Thermal Shock Test.

Comments:

LFS.01.11.09

Date Due: 12/11/01
Responsibility: Rockwell-Collins (Dave Hillman)
Required Action: Provide data to everyone showing the method by which tin whiskers form. This could be used to eventually develop a means of controlling tin whiskers.
Comments:

LFS.01.11.10

Date Due: 12/11/01
Responsibility: NASA/ITB (Brian Greene)
Required Action: Repair JTP. Incorporate comments received at the Nov 14-15 meeting into a strawman Repair JTP, and distribute it for review and comment.
Comments:

LFS.01.11.11

Date Due: 12/11/01
Responsibility: Rockwell-Collins (Dave Hillman)
Required Action: Test Board Design. Look into the possibility of having a vendor supply defective capacitors that are shorted.
Comments:

LFS.01.11.12

Date Due: 12/11/01
Responsibility: Boeing (Tom Woodrow)
Required Action: Test Board Design. Provide data from Lucent on the performance of immersion silver surface finish.
Comments:

LFS.01.11.13

Date Due: 12/11/01
Responsibility: Army (Martha Schuster)
Required Action: Test Board Design. Check the extent to which components are being soldered to flex boards in Army missiles and aviation
Comments:

LFS.01.11.14

Date Due: 12/11/01
Responsibility: Raytheon (Joe Felty, Jeff Bradford), Rockwell-Collins (Dave Hillman)
Required Action: Test Board Design. Prepare a list of the microelectronic devices proposed for the test board and the cost and availability of each.
Comments:

LFS.01.11.15

Date Due: 12/11/01
Responsibility: Air Force (Mark Stibitz)
Required Action: Repair JTP. Survey within Robins AFB to ascertain the percentage of solders that are high-temperature vs. low-temperature.
Comments:

LFS.01.11.16

Date Due: 11/26/01
Responsibility: All technical representatives
Required Action: CBA. Provide comments on suggested improvements to CTC's Cost Benefit Analysis data collection forms to CTC (Ron Patun).
Comments:

LFS.01.11.17

Date Due: 12/03/01
Responsibility: All technical representatives
Required Action: CBA. Anyone who might be interested in completing a Cost Benefit Analysis survey form should provide a point of contact to CTC (Ron Patun).
Comments:

LFS.01.11.18

Date Due: 12/11/01
Responsibility: Senju Metals (Derik Daily)
Required Action: PAR. Confirm with Senju's customers whether Sn/Ag/Cu and Sn/Ag/Cu/Bi solder alloys had been applied using wave solder.
Comments:

LFS.01.11.19

Date Due: 12/04/01
Responsibility: NASA/ITB (Brian Greene)
Required Action: Schedule a mid-December teleconference to discuss lead-free solder alternatives, the two JTPs, and the continuing work on test board design.
Comments:

Action Items Closed at this Meeting**LFS.01.11.02**

Date Due: 11/06/01
Responsibility: Raytheon (Joe Felty), NASA/ITB (Brian Greene)
Required Action: Prepare and distribute a meeting announcement, join-up instructions, and agenda for the November 14-15 meeting
Comments: 11/14/01 – Closed. Completed.

LFS.01.11.03

Date Due: 11/14/01
Responsibility: Raytheon (Joe Felty)
Required Action: Prepare a draft rationale for why each component is included on the proposed test board (e.g., its function, what data will be collected).
Comments: 11/14/01 – Closed. Test board design was discussed at 11/14 meeting and included in the meeting minutes

LFS.01.08.04

Date Due: 11/1/01 (originally 09/20/01)
Responsibility: AFRL (Dave Johnson)
Required Action: Have Larry Perkins put together an AFRL Science Advisory Board and report the results of the Board's first meeting at the next JG-PP lead-free solder project teleconference on 09/20/01.
Comments: 9/20/01 - In progress

Open Action Items**LFS.01.11.01**

Date Due: 12/09/01 (originally due 11/09/01)
Responsibility: NASA/ITB (Brian Greene)
Required Action: Each service and agency indicate to Brian Greene who will help in building a strawman depot level rework JTP. Build a skeletal framework of a Repair JTP for the November 14-15 meeting.
Comments: 11/09/01 – Names were provided to B. Greene. The strawman JTP has not been assembled yet, although a requirements matrix was developed by Mark Stibitz, Robins AFB. New due date for strawman Repair JTP is 12/09/01.

LFS.01.09.01

Date Due: 10/11/01
Responsibility: All project technical representatives
Required Action: Review and comment on the draft potential alternatives list, the draft JTP (especially details of the tests, such as vibration frequencies, dwell times, temperatures, ramp rates, etc.), and the test board design
Comments: 11/15/01 – Progress was made at the Nov 14-15 meeting. Awaiting input from more of the stakeholders.

LFS.01.08.01

- Date Due:** 11/1/01 (originally 08/22/01)
- Responsibility:** All Services and NASA [e.g., AFRL (Dave Johnson), TACOM (Carl Handsy), NAWCWD (John Nelson), USMC (Don Bowie), NASA (Bob Hill)]
- Required Action:** Itemize and describe any technical concerns your Service/organization has with use of lead-free solders. Distinguish concerns by new systems (manufacturing) versus old systems (depot repair).
- Comments:** 11/15/01 – Progress was made at the Nov 14-15 meeting. Awaiting input from more of the stakeholders.

LFS.01.08.02

- Date Due:** 11/1/01 (originally 08/22/01)
- Responsibility:** All Services and NASA [e.g., AFRL (Dave Johnson), TACOM (Carl Handsy), NAWCWD (John Nelson), USMC (Don Bowie), NASA (Bob Hill)]
- Required Action:** Identify the range of currently used lead-containing solder formulations and applications that the Services and NASA would be trying to replace (e.g., are they all eutectic [63% Sn/ 37% Pb]?).
- Comments:** 09/18/01 – WR-ALC indicates that 95% of their solders are 63Sn/37Pb. Awaiting more service input.

LFS.01.08.03

- Date Due:** 11/1/01 (originally 08/22/01)
- Responsibility:** All project technical representatives
- Required Action:** Review and comment on the suitability of the candidate lead-free solders that were emailed to the technical representatives on Tuesday, August 7. The information is contained in the four attached files. Brian Greene will consolidate all responses and provide them to all via e-mail within 2 weeks of final receipt (no later than 09/05/01).
- Comments:** 11/15/01 – Progress was made at the Nov 14-15 meeting. Awaiting input from more of the stakeholders.

LFS.01.06.03

- Date Due:** 10/11/01 (originally 07/30/01)
- Responsibility:** NAWCWD (John Nelson), Raytheon (Joe Felty), Rockwell-Collins (Dave Hillman)
- Required Action:** Identify (e.g., through a literature search) any lead-free and tin-lead solder interaction and report the findings at the next project meeting
- Comments:** 08/07/01 – Literature survey from John Nelson distributed to project representatives
- 09/20/01 – Action item amended to have CTC/NDCEE examine any interaction between Pb and Bi-containing solder alloys.

LFS.01.06.06

Date Due: 10/11/01 (originally 07/30/01)
Responsibility: All Technical Representatives
Required Action: Identify their top lead-free solder candidates to Joe Felty, Raytheon
Comments: 09/19/01 – Raytheon provided their recommendations; posted to the JG-PP Web site
11/15/01 – Progress was made at the Nov 14-15 meeting. Awaiting input from more of the stakeholders.

LFS.01.06.07

Date Due: 11/1/01 (originally 08/03/01)
Responsibility: All Technical Representatives
Required Action: Consolidate the candidate lead-free solders and provide them to CTC for inclusion in a draft JG-PP Potential Alternatives Report (PAR)
Comments: 11/15/01 – Progress was made at the Nov 14-15 meeting. At that meeting, a more refined list of alternatives was identified. Awaiting input from more of the stakeholders.